UM10456

QFN3333 demonstration board

Rev. 1 — 6 June 2011 **User manual**

Document information

Info	Content
Keywords	QFN3333, Point-Of-Load, demonstration board
Abstract	The QFN3333 demonstration board is a single-phase buck converter design for demonstrating the performance of NXP Semiconductors' QFN3333 MOSFETS in a small form factor Point-Of-Load (POL) circuit. The 3.3 cm × 6.1 cm (1.3 inch × 2.4 inch) four layer board converts 12 V nominal input to 1.2 V nominal output and is capable of a 25 A output current while maintaining a case temperature at or below 90 °C with a minimal 200 LFM (1 m/s) of airflow at 25 °C ambient. Efficiencies above 90 % are achieved at 12 V in/3.3 V out on this small demonstration board due to the superior on-resistance and thermal performance of the small footprint of the MOSFET S0T873 package.

Revision history

Rev	Date	Description
1	20110606	first issue

Contact information

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1. Introduction

The QFN3333 demonstration (demo) board demonstrates the performance of NXP Semiconductors' QFN3333 power MOSFETS in an operational single-phase buck converter on a small 3.3 cm × 6.1cm board. The innovative SOT873 package has a compact footprint of 3.3 mm × 3.3 mm enabling superior on-resistance and thermal performance by using an underside thermal pad electrically connected to the drain.

The low-cost board is designed to operate from an input voltage of 12 V (nominal) but is capable of operating from 5 V to 13 V. The board output voltage (V_O) is set by default to 1.2 V which can be adjusted from 0.8 V to 5 V by changing the value of an on-board resistor. The MOSFETs are rated at V_{DS} = 30 V. Specification details are available in the applicable MOSFET data sheet. These MOSFETs enable the board to provide continuous output currents of over 25 A using one control FET and two synchronizing FETs with adequate airflow.

Figure 1 shows the simplified outline and 3-D view of the QFN3333 package.

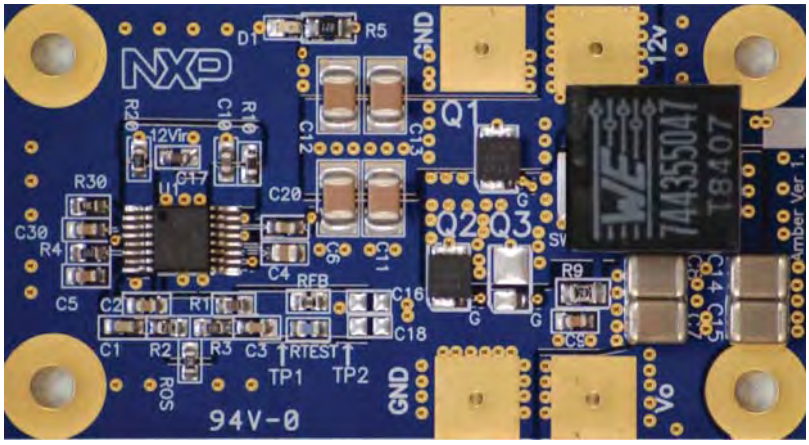
Fig 1. Simplified outline and 3-D view of the QFN3333 package

The Texas Instruments' TPS40077 controller was selected for its feature set which includes: voltage operating range of 4.5 V to 28 V, high-side current limit, source and sink drivers, and cross conduction protection. Technical information for the controller is available in the TPS40077 data sheet from Texas Instruments.

The board was designed as a simple low-cost reference design and is not intended to demonstrate the maximum performance achievable from the selected QFN3333 devices.

1.1 Demo board top and underside views

Figure 2 shows the top and underside view of the demo board. All components are located on the topside and are arranged with enough clearance to allow convenient attachment of meters and probes. Power input and output connections and mounting hole pad positions are mirrored on top and underside.



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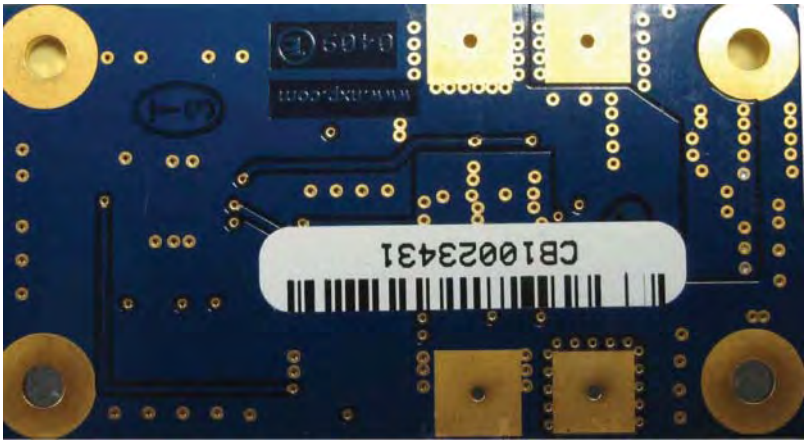
a. Top view



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b. Bottom view

Fig 2. Demo board top and underside views

1.1.1 Connection details

Figure 3 shows the board connections. Input power and ground connection pads are located on the top of the board, and output power and ground connection pads are located on the underside of the board. The pads are large and their positions are mirrored on the board top and underside for improved current handling capability. Solder connections or clips can be used to attach power. Voltage drop can be reduced by soldering connections to the pads. Small holes in the input and output pads are sized so conductive posts can be inserted for oscilloscope and meter probes. Mounting holes in the corners of the board are connected to ground.

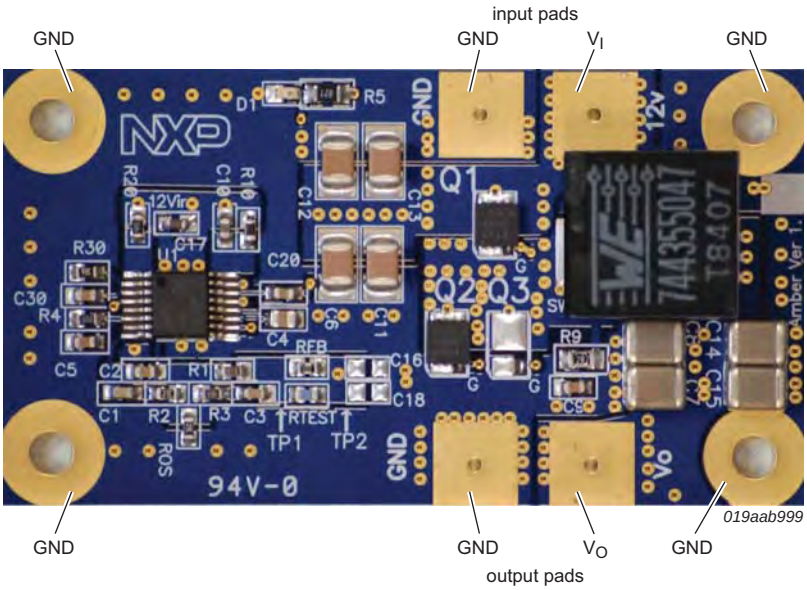


Fig 3. Demo board input and output pads

2. Design criteria

The board is supplied with the output set to 1.2 V at 25 A. The output voltage can be changed by replacing a resistor as explained in Section 2.1. At an output of 1.2 V, the current limits are set for 25 A; see Table 1. The operating frequency is fixed at 500 kHz. A blue status LED at the top of the board lights when the controller and board are operating. The 400 nH inductor is a 30 A device (100 °C), with a soft saturation curve and was selected to provide good efficiency due to its low 0.9 mΩ DCR.

2.1 Board features

The output voltage can be easily adjusted by changing the value of a single resistor. The current limit can also be adjusted as described in Section 2.1.2. If V_O is changed the current limit must also be adjusted to maintain a constant current limit. The feedback path has been designed so that phase/gain testing can be performed by removing a single resistor. A brief description of these features is provided in the following sections.

2.1.1 V_O selection

Replacing R_{OS} with the values calculated in Equation 1 changes the output voltage (V_O).

$$R_{OS} = R1 \times \frac{V_S}{V_O - V_S} \quad (1)$$

Where V_S is the error amplifier reference voltage; it is fixed at 0.7 V for the TPS40077. Resistor values for common output voltages are given in Table 1.

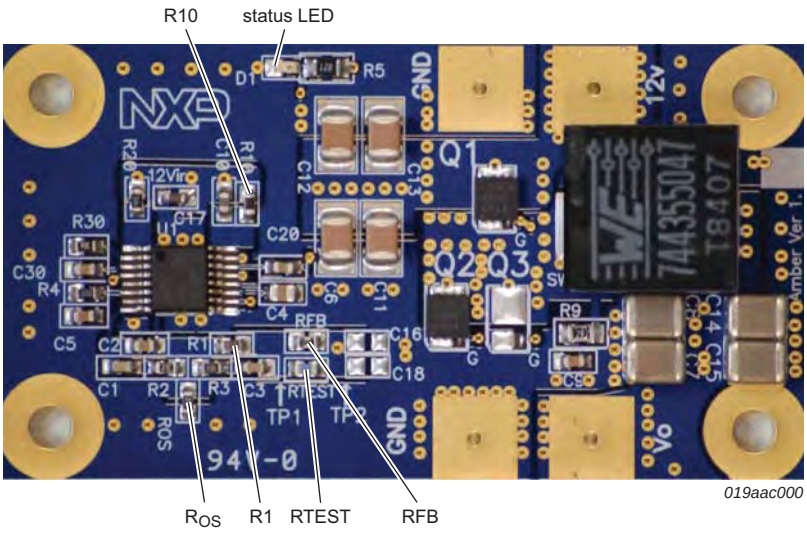


Fig 4. Location of R_{OS}

2.1.2 Control FET current limit

The TPS40077 data sheet discusses the parameters affecting the value of R10 for a desired current limit. The voltage drop across R10 (VR10) is compared with the voltage drop across the control FET at full conduction, and initiates a shutdown if the FET exceeds VR10. The FET voltage drop is affected by the nominal values of V_O/V_I, temperature, and output current. FET voltage drop is a direct function of drain-source on-state resistance (R_{DSon}), and thus is temperature dependent. The blue LED will flicker during current limit shutdown. Please refer to the TPS40077 data sheet for additional information on current limit settings.

The demo board is shipped with an R10 value of 1180 Ω, typically initiating a current limit shutdown for currents exceeding 25 A, (case temperatures ≤ 90 °C, V_I = 12 V). For other V_O and V_I values, R10 must be changed to provide this thermal protection. The table below should assist in the selection. There may be variations in shutdown current between demo boards, because of variation in R_{DSon} between FETs.

Table 1. Shutdown current limit

V_O (V)	R_{OS} (kΩ)	R10 for V_I = 12 V	R10 for V_I = 10 V	R10 for V_I = 8 V	Shutdown I_O (A)
0.8	60.4	634	832	1180	28
1.2	12.1	1180	1540	1904	25
1.5	7.32	1400	1820	2260	22
2.5	3.32	2370	2670	2740	18
3.3	2.32	2940	3090	3090	16
5.0	1.40	2610	2610	2610	14

2.1.3 Phase/gain testing

Phase/gain testing (Bode plots) can be performed by removing the RFB resistor and injecting a test signal across a 50 Ω resistor (RTEST) as shown in Figure 5. By monitoring the response at TP2 to the injected signal at TP1, a phase/gain plot can be generated by varying the frequency of the test signal. The full details of this test are beyond the scope of

this manual, however the measurements are easily made using a Vector Network Analyzer (VNA). Please refer to the TPS40077 data sheet for loop compensation techniques. The RFB resistor should remain in the circuit for normal operation.

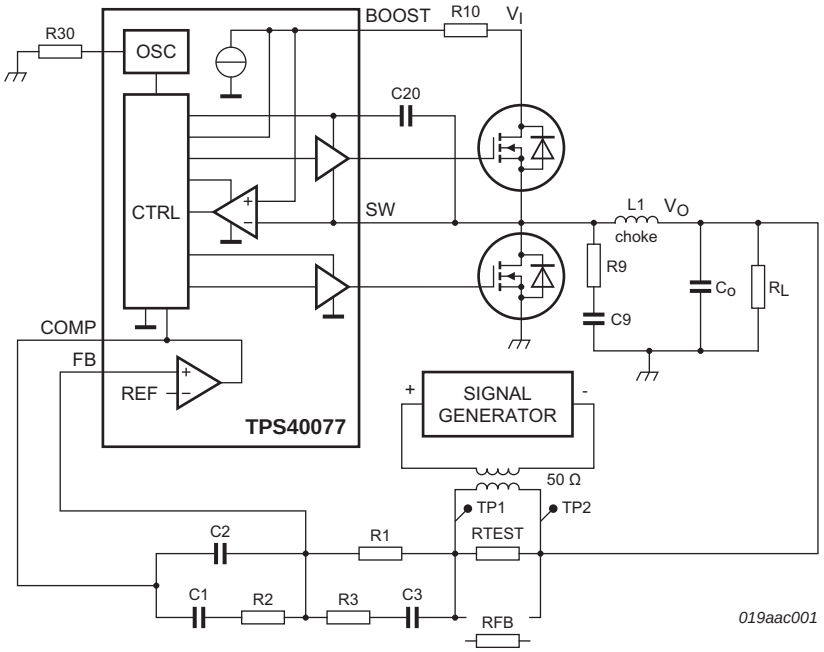
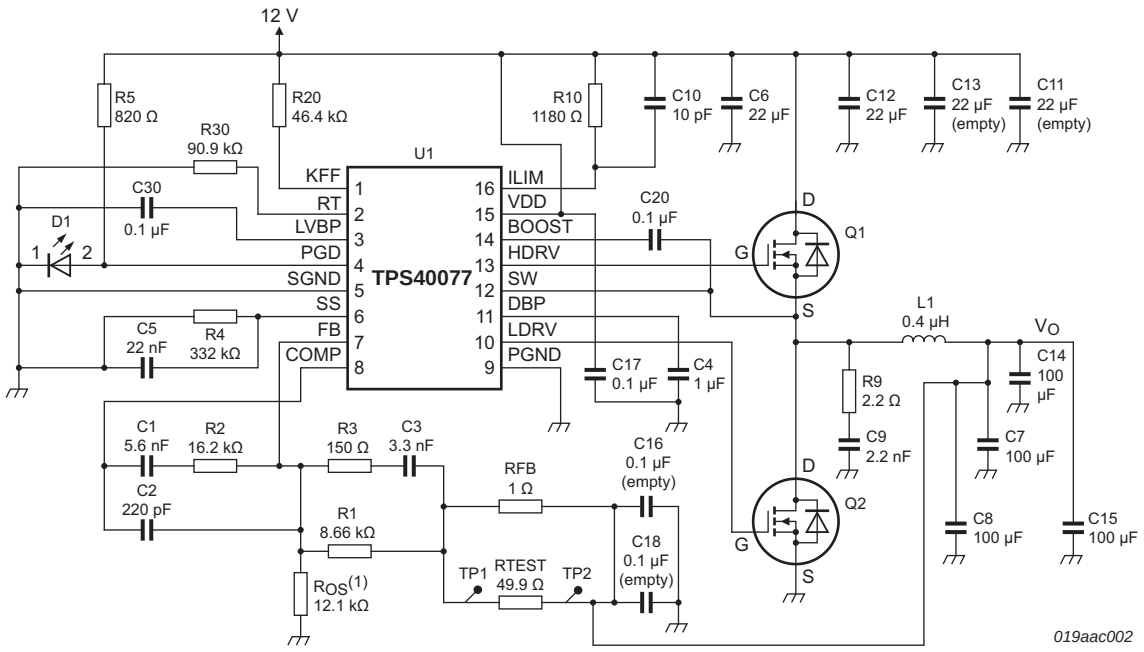


Fig 5. Phase/gain test setup

2.2 Board schematic

The board schematic is shown in Figure 6.

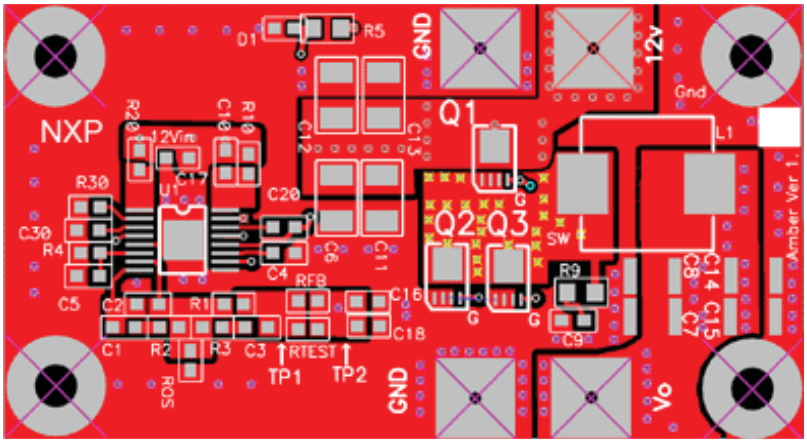


(1) R_{OS} is set for V_O = 1.2 V; reference voltage = 0.7 V.

Fig 6. Demo board schematic

2.3 Layout

The demo board is constructed using four layers. All layers are plated with one-ounce copper. All signals are routed top and underside, with the inner power and ground layers as shown in Figure 7. The board was designed to minimize high current-induced noise in the input drive and controller circuit areas. The input current flows in a tight loop between the input pads, the input decoupling capacitors and the MOSFETs. The output current is also confined to a separate loop. The controller is placed outside either of these high noise power paths. High current paths are separated from sensitive circuit areas by power-plane splits. The ground plane is not split but uses careful component placement to keep switching-current noise away from sensitive circuit areas.



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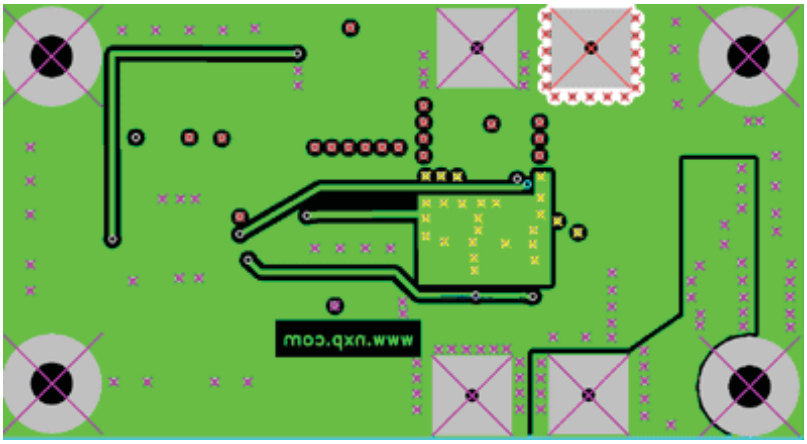
a. Top layer



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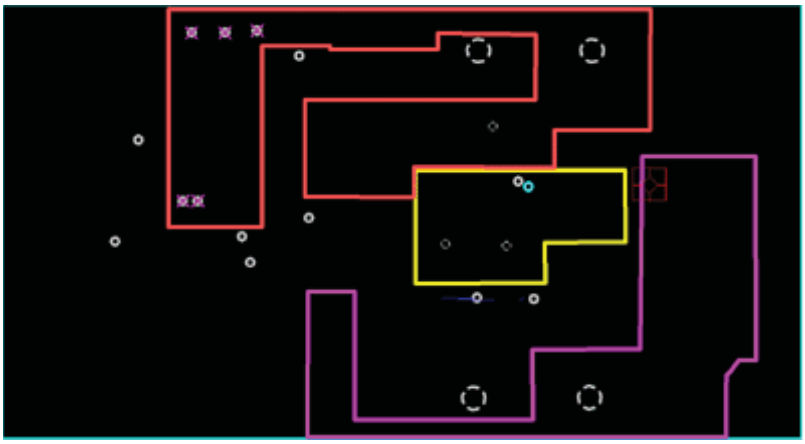
b. Bottom layer



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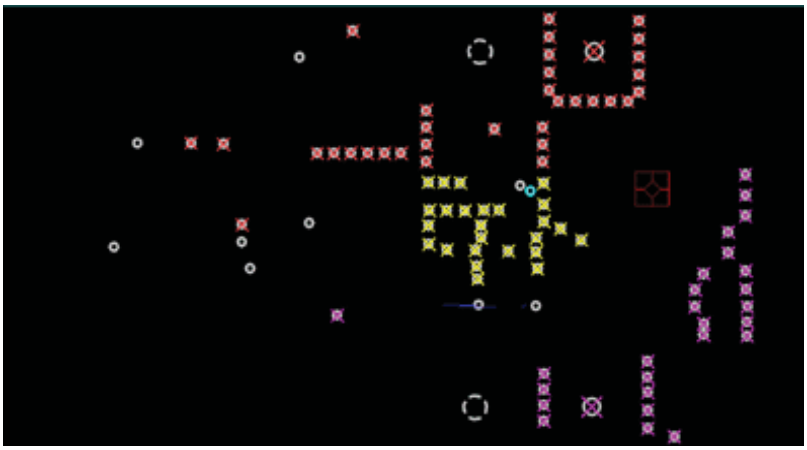
c. Power layer



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d. Ground layer

Fig 7. Demo board layouts

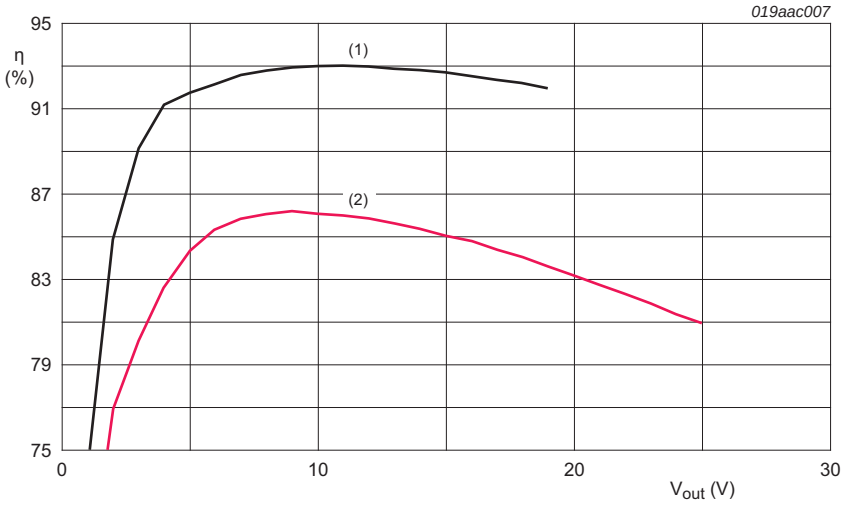
3. Electrical and thermal performance

The demo board is designed to manage output currents of 25 A with V_O set to 1.2 V (30 W) and 18 A with V_O set to 3.3 V (76 W). This rating is based on a 90 °C case temperature limit at 25 °C ambient and 200 LFM (1 m/s) airflow.

3.1 Efficiency sweeps

Efficiency is plotted in Figure 8 for V_O voltages of 1.2 V and 3.3 V. The input voltage is 12 V for both sweeps. The maximum current swept is the level that produces 90 °C FET case temperatures. Higher currents can be achieved with greater airflow. If higher currents are desired, the current limit set-point will need to be adjusted by changing the value of R10.

The power output increases directly with V_O for a constant current output. The loss factors do not increase as fast, making conversion to higher V_O values more efficient than conversion to lower V_O values.



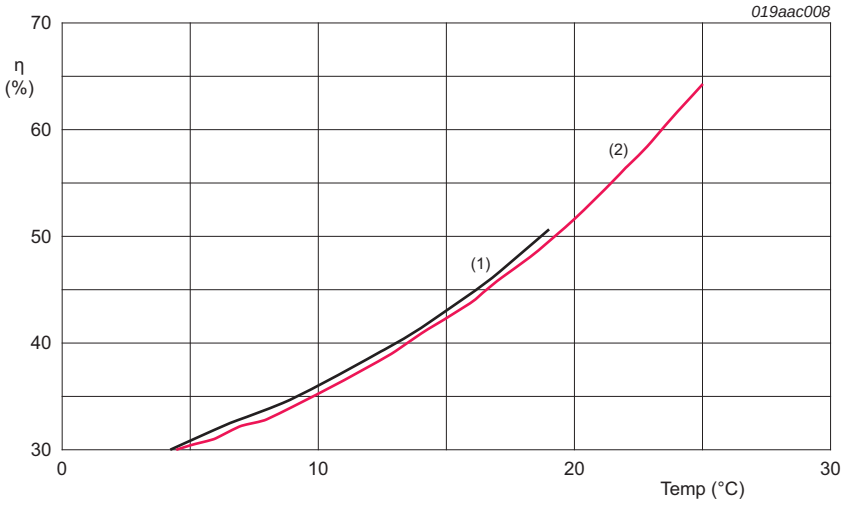
(1) 3.3 V efficiency.

(2) 1.2 V efficiency.

Fig 8. Efficiency sweeps

3.2 Thermal sweeps

Figure 9 shows the thermal case temperature of the control and synchronizing FETs for the efficiency sweeps in Figure 8. The load current is swept from almost zero amplitude to a maximum level, which is defined when the average of the two case temperatures equals 90 °C.



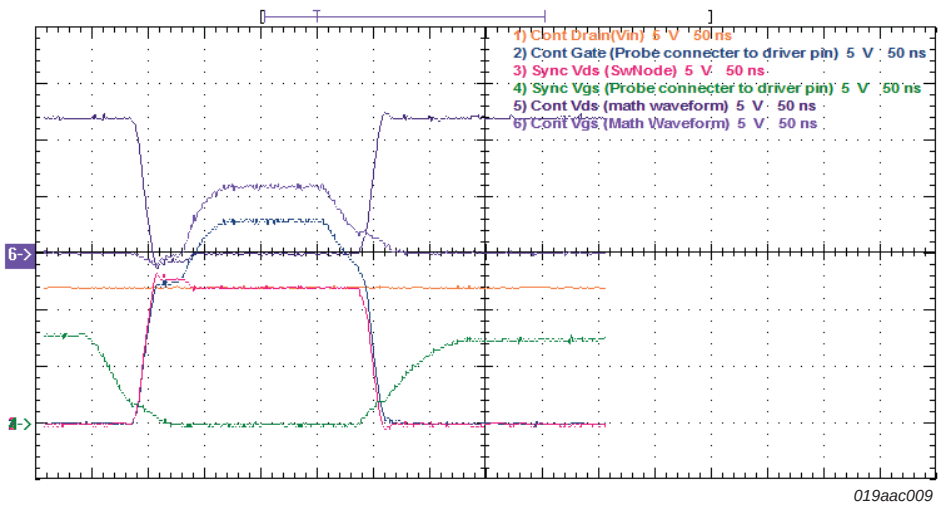
(1) 3.3 V temperature.

(2) 1.2 V temperature.

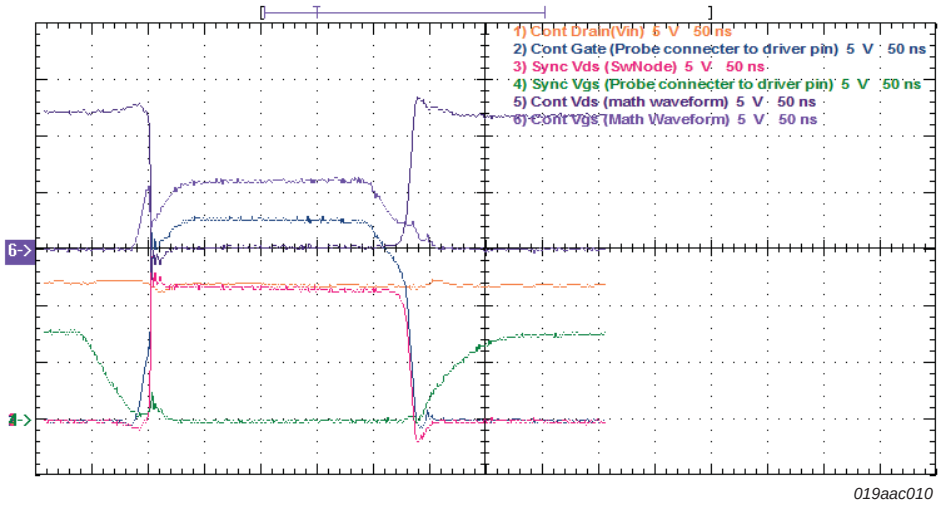
Fig 9. Thermal measurement for 12 V input

3.3 Electrical waveforms

The oscilloscope plots in Figure 10 show the synchronizing FET gate, control FET gate, switch node, at no load and 22 A load respectively.



a. I_O = 0 A



b. I_O = 22 A

Fig 10. Waveforms at V_I = 12 V; V_O = 1.2 V; 500 kHz

3.4 Loop gain phase plot

Figure 11 shows the loop gain and phase as a function of frequency for V_O = 1.2 V. The results were nearly the same for V_O ranges of 0.8 V to 3.3 V. The test setup is shown in Figure 5.

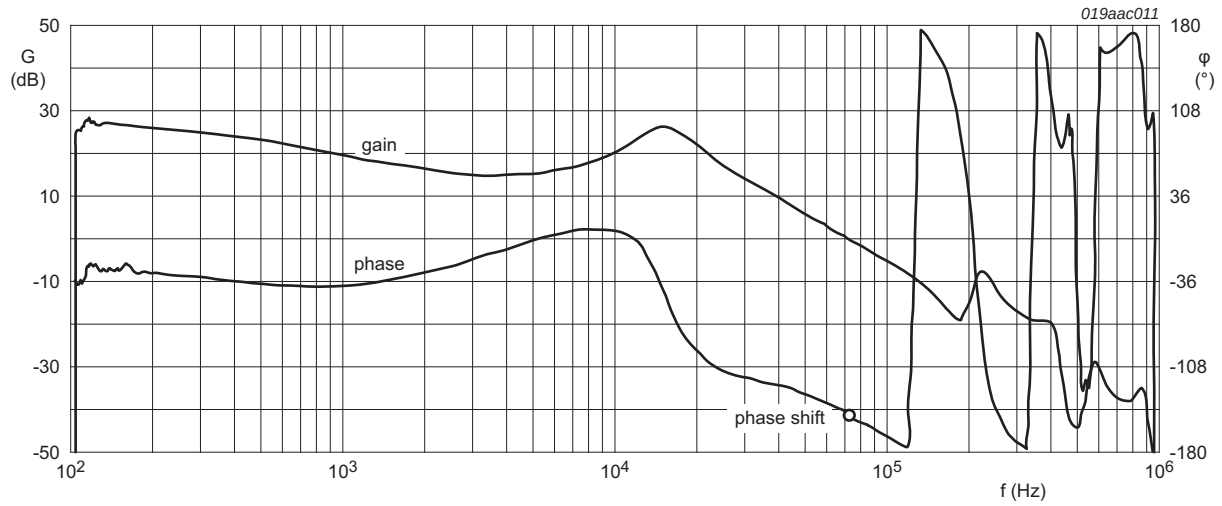


Fig 11. Demo board phase and gain curves

4. Bill of materials

Table 2. Demonstration board BOM

Reference	Qty	Package	Item	Value	Tolerance	Rating	Manufacturer and part number
C3	1	603	1	3.3 nF	±10 %	50 V	TDK
C10	1	603	2	10 pF	±10 %	50 V	TDK
C2	1	603	3	220 pF	±10 %	50 V	TDK
C9	1	603	4	2.2 nF	±10 %	50 V	TDK
C5	1	603	5	22 nF	±10 %	50 V	TDK
C1	1	603	6	5.6 nF	±10 %	50 V	TDK
C12, C20, C30, (C16, C18 empty)	5	603	7	0.1 μF	±10 %	50 V	TDK
C4	1	805	8	1 μF	±10 %	16 V	TDK
C6, C12, (C11, C13 empty)	4	1210	9	22 μF	+80 % to −20 %	16 V	TDK
C7, C8, C14, C15	4	1812	10	100 μF	+80 % to −20 %	6.3 V	TDK
R30	1	603	11	90.0 kΩ	±1 %	-	-
R1	1	603	12	8.66 kΩ	±1 %	-	-
R4	1	603	13	332 kΩ	±1 %	-	-
R10	1	603	14	1180 kΩ	±1 %	-	-
R2	1	603	15	16.2 kΩ	±1 %	-	-
R_{OS}	1	603	16	12.1 kΩ	±1 %	-	-
R20	1	603	17	46.4 kΩ	±1 %	-	-
R3	1	603	18	150	±1 %	-	-
RTEST	1	603	19	49.9	±1 %	-	-
R9	1	805	20	2.2	±5 %	-	-

Table 2. Demonstration board BOM

Reference	Qty	Package	Item	Value	Tolerance	Rating	Manufacturer and part number
R5	1	805	21	820	±5 %	-	-
RFB	1	603	22	1	±1 %	-	-
U1	1	SOP	23	TPS40077	-	-	TI; TPS40077PWP
Q1	1	QFN3333	24	Control	-	-	NXP; Control
Q2	1	QFN3333	25	Sync	-	-	NXP; Sync
D1	1	603	26	Blue LED	-	3.8 V	Lite-On; LTST-C190UBKT
L1	1	WE-HC/HCA 13 ×13	27	744355047	±20 %	0.47 μH	WURTH; 744355047

5. Abbreviations

Table 3. Abbreviations

Acronym	Description
BOM	Bill Of Materials
DCR	Direct Current Resistance
LFM	Linear Feet per Minute

6. References

[1] **TPS40077 —** Texas Instruments data sheet: High-efficiency, midrange-input synchronous buck controller with voltage feed-forward.

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